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DESCRIPTION

SEMICONDUCTOR DEVICE

TECHNICAL FIELD

The present invention relates to a semiconductor device and, more particularly, to a semiconductor device provided with a power supply voltage variation detection circuit which detects steep variations of the voltage difference between the power supply voltage and the reference voltage.

BACKGROUND ART

Hereinafter, a conventional semiconductor device provided with a power supply variation detecting circuit will be described with reference to figure 11(refer to Patent Reference No.1). As shown in figure 11, the semiconductor device is provided with two resister elements 103-106 between the power supply terminal 101 and the ground terminal 102. Further, it is provided with two-input comparators 107, 108. The comparator 107 receives an input from an one side input terminal that is obtained by dividing the power supply voltage 109 by the resister elements 105 and 106, and receives the reference voltage 112 from the other side input terminal. Further, there is provided a capacitance element 118 between a signal line connecting the one side terminal of the comparator 107 and the node 113 and the power supply terminal 116. Further, there is provided a logic AND circuit 119 operating output signals of the comparator 107, 108.

In the semiconductor device constituted as above, by comparing the divided power supply voltage 109 and the reference voltage 110 by the comparator 107, variations at positive side of the power supply voltage is detected, and by comparing the divided power supply voltage 111 and the reference voltage 112, variations at negative side of the power supply voltage is detected. When the power supply voltage varies toward the positive side, the voltage variations are capacitance-coupled by the capacitance element 117, and thereby the power supply voltage which is inputted to the one side input of the comparator 107 is varied, thereby becoming a reference voltage. The comparator 107 detects the voltage difference, and outputs a signal indicating that effect. Similarly, when the power supply voltage varies toward the negative side, the comparator 108 detects the voltage difference, and outputs a signal indicating that effect. The output signals of the comparators 107, and 108 are calculated by the logic AND circuit 119. By such a construction, the semiconductor device can output a logic signal indicating that the power supply voltage variation is detected.

Further, another conventional semiconductor device which is provided with a power supply voltage variation detection circuit will be described with reference to figure 12(Patent Reference No.2). In this semiconductor device, there are two inverter circuits 201, 202 which receive power supply voltage

and ground voltage as inputs, and the output of the first stage inverter circuit 201 and the input of the second stage inverter circuit 202 are connected via the integration delay circuit comprising the resister element 203 and the capacitance element 204, and the output of the second stage inverter circuit 202 is connected to the input of the first stage inverter circuit 201. Thereby, when the voltage difference between the power supply voltage and the ground voltage varies steeply, the initial value which is previously stored is reversed, thereby outputting a logic signal indicating a steep increase or fall down of the voltage difference.

Patent reference No.1: EP1160580A1

Patent reference No.2: Japanese Published Patent Application Hei.6-152358(page7, Figure 3)

DISCLOSURE OF THE INVENTION

THE PROBLEMS TO BE SOLVED BY THE INVENTION

In the prior art semiconductor device described above, there is a problem that the detection level of the steep power supply voltage variation depends on the voltage value before voltage variation, i.e., the power supply voltage value at a normal state. For example, in the semiconductor device shown in figure 11, when the voltage variation at negative side is detected, if the power supply voltage value before the variation is low, only a small voltage variation by slight noises are detected as abnormal, and therefore, there is a possibility that

the voltage variation which would not affect the operation of the semiconductor device should be detected as abnormal. In addition, when the power supply voltage before variations is high, there is a possibility that abnormality is detected only when a relatively large voltage variation arises.

Also for the semiconductor device shown in figure 12, there are similar problems as in the semiconductor device shown in figure 11, because the detection level of the power supply voltage variation depends on the voltage value before the voltage variation occurs.

From the above, in the prior art semiconductor device, it is necessary to consider not only the variation of the power supply voltage but also the value of the power supply voltage before variation when designing a circuit for detecting the power supply voltage variations. This results in a lot of parameters to be considered in designing, and also it has also become difficult in a circuit designing.

Therefore, it is an object of the present invention to provide a semiconductor device provided with a circuit for detecting variations in the power supply voltage, which can detect steep variations in the power supply voltage without depending on the power supply voltage before the voltage variations.

MESURES TO SOLVE THE PROBLEMS

In order to solve the above-described problems, there is

provided a semiconductor device according to Claim 1 of the present invention which comprises: a first comparator which has two input nodes having opposite polarity to each other and receives a reference voltage and a power supply voltage at their inputs to compare the respective voltage values to output a signal indicating a comparison result; a first resister element which connects the one side input node and the other side input node of the first comparator; a capacitance element one end of which is connected to a power supply terminal which applies said power supply voltage and the other end of which is connected to the one side input node of the comparator; and the first comparator activates the output signal indicating the comparison result when the voltage difference between the reference voltage and the power supply voltage varies.

A semiconductor device according to Claim 2 of the present invention comprises, in a semiconductor device as defined in claim 1, the first comparator comprising a hysteresis comparator which activates the output signal indicating the comparison result when the voltage difference between the reference voltage and the power supply voltage becomes larger than a predetermined hysteresis width.

A semiconductor device according to claim 3 of the present invention comprises, in a semiconductor device as defined in claim 1, further a second and a third resister element connected in series between the power supply terminal and the ground

terminal to divide the power supply voltage; a second comparator having two input nodes and receives the power supply voltage divided by the second and the third resister element and the reference voltage at its inputs to compare those; and a logic OR circuit which takes a logic OR operation of the output signal of the first comparator and the output signal of the second comparator.

A semiconductor device according to claim 4 of the present invention comprises, in a semiconductor device as defined in any of claims 1 to 3, further a reset portion which receives the output signals of the first comparator or the logic OR circuit at their inputs, and stops the operation of the system including the semiconductor device when the output signal of the first comparator or the output signal of the second comparator is activated.

A semiconductor device according to claim 5 of the present invention comprises, in a semiconductor device as defined in any of claims 1 to 3, further a switching part which switches the value of the power supply voltage which is inputted to either of the input nodes of the first comparator to an arbitrary value.

A semiconductor device according to claim 6 of the present invention comprises, in a semiconductor device as defined in claim 5, further a control section which operates the switching part at turning on the power of the semiconductor device.

A semiconductor device according to claim 7 of the present

invention comprises: a first and a second comparators each of which has two input nodes having opposite polarity to each other and receives a reference voltage and a power supply voltage at their inputs to compare the respective voltage values to output a signal indicating a comparison result; a first and a second resister elements each of which connects the one side input node and the other side input node of the first and the second comparators, respectively; a first and a second capacitance elements, one end of which is both connected to a power supply terminal which applies said power supply voltage, and the other end of which is connected to the one side input node of the first and the second comparator, respectively; a logic OR circuit which takes a logic OR operation of the output signal of the first comparator and the output signal of the second comparator: the first and the second comparators respectively activate the output signal indicating the comparison results when the voltage difference between the reference voltage and the power supply voltage varies, and the polarity of the input node which receives the power supply voltage in the first comparator and the polarity of the input node which receives the power supply voltage in the second comparator are opposite to each other.

A semiconductor device according to claim 8 of the present invention comprises, in a semiconductor device as defined in claim 7, further the first comparator and the second comparator being hysteresis comparators which activates the output signal

indicating the comparison result when the voltage difference between the reference voltage and the power supply voltage is larger than a predetermined hysteresis width. Thereby, the variations in the power supply voltage which do not affect the operation of the semiconductor device may not be erroneously detected as abnormal voltage variation.

A semiconductor device according to claim 9 of the present invention comprises, in a semiconductor device as defined in claim 7, further a third and a fourth resister elements connected in series between the power supply terminal and the ground terminal to divide the power supply voltage, and a third comparator which has two input nodes and compares the power supply voltage which is divided by a third and a fourth resister elements and the reference voltage to output a signal indicating the comparison result to the logic OR circuit.

A semiconductor device according to claim 10 of the present invention comprises, in a semiconductor device as defined in any of claims 7 to 9, further a reset part which receives the output signal of the logic OR circuit at its input and stops the operation of a system including the semiconductor device when the output signal of the first comparator, the second comparator, or the third comparator is activated.

A semiconductor device according to claim 11 of the present invention comprises, in a semiconductor device as defined in claims 7 to 9, further a switching part which switches

the value of the power supply voltage which is inputted to either of the input nodes of the first and the second comparators to an arbitrary value.

A semiconductor device according to claim 12 of the present invention comprises, in a semiconductor device as defined in claim 11, further a control section which operates the switching part at turning on the power of the semiconductor device.

EFFECTS OF THE INVENTION

Since in order to solve the above-described problems, a semiconductor device according to Claim 1 of the present invention which comprises: a first comparator which has two input nodes having opposite polarity to each other and receives a reference voltage and a power supply voltage at their inputs to compare the respective voltage values to output a signal indicating a comparison result; a first resister element which connects the one side input node and the other side input node of the first comparator; a capacitance element one end of which is connected to a power supply terminal which applies said power supply voltage and the other end of which is connected to the one side input node of the comparator; and the first comparator activates the output signal indicating the comparison result when the voltage difference between the reference voltage and the power supply voltage varies, the voltage variations can be detected irregardless of the power supply voltage value before

the voltage variations. As a result, with relative to the prior art semiconductor device, the parameters which should be considered on designing are reduced, and the circuit design is simplified.

Since the semiconductor device according to Claim 2 of the present invention comprises, in a semiconductor device as defined in claim 1, the first comparator comprising a hysteresis comparator which activates the output signal indicating the comparison result when the voltage difference between the reference voltage and the power supply voltage becomes larger than a predetermined hysteresis width, the variations in the power supply voltage which does not affect on the operation of the semiconductor device may not be erroneously detected as abnormal voltage variations.

Since a semiconductor device according to claim 3 of the present invention comprises, in a semiconductor device as defined in claim 1, further a second and a third resister element connected in series between the power supply terminal and the ground terminal to divide the power supply voltage; a second comparator having two input nodes and receives the power supply voltage divided by the second and the third resister element and the reference voltage at its inputs to compare those; and a logic OR circuit which takes a logic OR operation of the output signal of the first comparator and the output signal of the second comparator, not only the steep voltage variations but

also smoothly varying voltage variations can be detected.

Since a semiconductor device according to claim 4 of the present invention comprises, in a semiconductor device as defined in any of claims 1 to 3, further a reset portion which receives the output signals of the first comparator or the logic OR circuit at their inputs, and stops the operation of the system including the semiconductor device when the output signal of the first comparator or the output signal of the second comparator is activated, even if attacks such as falsification of data or unjustified reading out is carried out by steeply changing the power supply voltage, this is automatically detected to conduct a reset and thus it is possible to take countermeasures against such attacks.

Since a semiconductor device according to claim 5 of the present invention comprises, in a semiconductor device as defined in any of claims 1 to 3, further a switching part which switches the value of the power supply voltage which is inputted to either of the input nodes of the first comparator to an arbitrary value, it is possible t confirm whether the comparator is operating normally.

Since a semiconductor device according to claim 7 of the present invention comprises: a first and a second comparators each of which has two input nodes having opposite polarity to each other and receives a reference voltage and a power supply voltage at their inputs to compare the respective voltage values

to output a signal indicating a comparison result; a first and a second resister elements each of which connects the one side input node and the other side input node of the first and the second comparators, respectively; a first and a second capacitance elements, one end of which is both connected to a power supply terminal which applies said power supply voltage, and respective the other end of which is connected to the one side input node of the first and the second comparator, respectively; a logic OR circuit which takes a logic OR operation of the output signal of the first comparator and the output signal of the second comparator: the first and the second comparators respectively activate the output signal indicating the comparison results when the voltage difference between the reference voltage and the power supply voltage varies, and the polarity of the input node which receives the power supply voltage in the first comparator and the polarity of the input node which receives the power supply voltage in the second comparator are opposite to each other, the voltage variations at positive side and at the negative side can be detected without dependent on the power supply voltage value before the voltage variation. As a result, with relative to the prior art device, the parameters which should be considered in designing can be reduced, and the circuit designing is eased.

Since a semiconductor device according to claim 8 of the present invention comprises, in a semiconductor device as

defined in claim 7, further the first comparator and the second comparator being hysteresis comparators which activates the output signal indicating the comparison result when the voltage difference between the reference voltage and the power supply voltage is larger than a predetermined hysteresis width, it may not occur that variations in the power supply voltage which do not affect the operation of the semiconductor device should be erroneously detected as abnormal voltage variation. Or it may not occur that variations in the power supply voltage which do not affect on the operation of the semiconductor device should be erroneously detected as abnormal voltage variation.

Since a semiconductor device according to claim 9 of the present invention comprises, in a semiconductor device as defined in claim 7, further a third and a fourth resister elements connected in series between the power supply terminal and the ground terminal to divide the power supply voltage, and a third comparator which has two input nodes and compares the power supply voltage which is divided by a third and a fourth resister elements and the reference voltage to output a signal indicating the comparison result to the logic OR circuit, not only the steep voltage variations but also smoothly varying voltage variations can be detected.

Since a semiconductor device according to claim 10 of the present invention comprises, in a semiconductor device as defined in any of claims 7 to 9, further a reset part which

receives the output signal of the logic OR circuit at its input and stops the operation of a system including the semiconductor device when the output signal of the first comparator, the second comparator, or the third comparator is activated, even when attacks such as falsification of data or unjustified reading out is carried out by steeply changing the power supply voltage, this is automatically detected to conduct a reset and thus it is possible to take countermeasures against such attacks.

Since a semiconductor device according to claim 11 of the present invention comprises, in a semiconductor device as defined in claims 7 to 9, further a switching part which switches the value of the power supply voltage which is inputted to either of the input nodes of the first and the second comparators to an arbitrary value, it is possible to confirm whether the comparator is operating normally.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a diagram illustrating a circuit construction of a semiconductor device according to a first embodiment of the present invention.

Fig.2 is a diagram showing a timing chart exemplifying the operation of the semiconductor device according to the first embodiment of the present invention.

Fig.3 is a diagram illustrating a circuit construction of a semiconductor device according to a second embodiment of

the present invention.

Fig.4 is a diagram showing a timing chart exemplifying the operation of the semiconductor device according to the second embodiment of the present invention.

Fig.5 is a diagram showing gain characteristics of the FIR filter when a weighting value n is changed.

Fig.5 is a diagram illustrating a circuit construction of a semiconductor device according to a third embodiment of the present invention.

Fig.6 is a diagram showing a timing chart exemplifying the operation of the semiconductor device according to the third embodiment of the present invention.

Fig.7 is a diagram illustrating a circuit construction of a semiconductor device according to a fourth embodiment of the present invention.

Fig.8 is a diagram showing a timing chart exemplifying the operation of the semiconductor device according to the fourth embodiment of the present invention.

Fig.9 is a diagram illustrating a circuit construction of a semiconductor device according to a fifth embodiment of the present invention.

Fig.10 is a diagram showing a timing chart exemplifying the operation of the semiconductor device according to the fifth embodiment of the present invention.

Fig.11 is a diagram illustrating a circuit construction

of a prior art semiconductor device having a power supply voltage variation detecting circuit.

Fig.12 is a diagram illustrating a circuit construction of a prior art semiconductor device having a power supply voltage variation detecting circuit.

DESCRITION OF NUMERALS

1, 11 comparator

2, 8, 12, 13 resister element

3, 9 capacitance element

4 power supply terminal

5 input terminal of a reference voltage

6, 7 hysteresis comparator

10, 14 logic OR circuit

15 switching part

16 inverter

17 p channel transistor

18 n channel transistor

IN1 input terminal of an arbitrary power supply voltage

N1, N2, N7, N8 input terminals of the comparators

N3 ~ N6 input terminals of the hysteresis comparators

Y1 ~ Y5 detected signal

101, 115, 115 power supply terminal

102 ground terminal

103, 104, 105, 106, 203 resister element

107, 108 comparator

109, 111 divided voltage

110, 112 reference voltage

117, 118, 204 capacitance element

119 logic AND circuit

201, 202 inverter

205 input line

206 output line

207 power supply voltage variation detection outputting line

BEST MODE FOR EMBODING THE INVENTION

Hereinafter, preferred embodiments of the present invention will be described with reference to the drawings.

(Embodiment 1)

A semiconductor device according to a first embodiment of the present invention will be described with reference to figures 1 and 2.

Figure 1 is a diagram illustrating a circuit construction of a semiconductor device according to a first embodiment of the present invention. The semiconductor device shown in figure 1 includes a comparator 1, a resister element 2, and a capacitor element 3. The comparator 1 has two input terminals (input terminals N1 and N2), and receives the reference voltage and the power supply voltage at its inputs and compares those. The resister element 2 connects between the signal line L1 which is connected to the input terminal N1 and the signal line L2 which is inputted to the input terminal N2 of the comparator

1. The capacitor element 3 has its one side end which is connected to the power supply terminal 4 and its other side end which is connected to one side input terminal (input terminal N1) of the comparator 1. The input terminal 5 of the reference terminal is connected to the other side input terminal (input terminal N2) of the comparator 1 via the signal line L2.

Besides, in figure 1, both of the input terminal N1(N2) and the signal line L1(L2) which is connected thereto may be considered as input nodes, and only the input terminal N1(N2) may be considered as input nodes. Accordingly, the resister element 2 may be connected between the input terminals N1, N2 of the comparator 1 only via either one of the signal lines L1 and L2, or it may be directly connected between the input terminals N1, N2.

The operation of the semiconductor device constructed as above, will be described with reference to figure 2. Figure 2 is a timing chart exemplifying the operation of the semiconductor device shown in figure 1. In figure 2, VDD denotes a power supply voltage, VREF denotes a reference voltage, and Y1 denotes a detection signal which is an output of the comparator 1.

First of all, at time t0, a power supply voltage VDD is applied to the power supply voltage terminal 4, and a reference voltage VREF is applied to the input terminal 5 of the reference voltage. Then, the voltages which are inputted to the input

terminals N1, N2 of the comparator 1 are equal to each other by the resister element 2.

Next, it is supposed that a positive side voltage variation is generated at the power supply voltage VDD during from time t1 to time t2. Then, the voltage variation component is capacitance-coupled by the capacitance element 3, and thereby the voltage which is inputted to the input terminal N1 of the comparator 1 also varies to become a voltage higher than the reference voltage VREF. This voltage difference is amplified by the comparator 1 to make the detected signal Y1 transit from low level to high level, and thereby a high level detected signal Y1 is outputted. This high level detected signal Y1 is inputted to the reset part (not shown), and this reset part stops the operation of the whole system including the semiconductor device(for example, an LSI). Accordingly, even if attacks such as falsification of data or unjustified reading out is carried out by steeply changing the power supply voltage, this is automatically detected to conduct a reset and thus it is possible to take countermeasures against such attacks. Also, this detection can be carried out without depending on the power supply voltage value before the power supply voltage variation.

As described above, a semiconductor device according to the first embodiment of the present invention can provide the following effects. That is, while in the prior art

semiconductor device the detection level of the voltage variation depends on the power supply voltage value because the power supply voltage which was divided by the resister elements is simply compared with the reference voltage, in the semiconductor device according to the first embodiment of the present invention, the detection level of the voltage variation does not depend on the power supply voltage value before the voltage variation because the voltage variation from the state where the reference voltage and the power supply voltage value is made the same value by the resister element 2. As a result, with relative the prior art semiconductor device, parameters which should be considered in designing are reduced, and the circuit design is eased.

While in the above-described first embodiment the operation of detecting the voltage variation at positive side is detected, the voltage variation at negative side can also detected by making the polarity of the input terminal N1 and the input terminal N2 of the comparator 1 reverse to each other, i.e., making the input terminal N1 a reverse phase input terminal (hereinafter referred to as "- terminal") and making the input terminal N2 as a positive phase input terminal (hereinafter referred to as a "+ terminal").

(Embodiment 2)

A second embodiment of the present invention will be described with reference to figures 3 and 4. Figure 3 is a

diagram illustrating a circuit construction of a semiconductor device according to the second embodiment of the present invention. The semiconductor device shown in figure 3 is characterized in that a hysteresis comparator 6 is provided in place of a comparator 1 in the semiconductor device shown in figure 1. Besides, the components similar to those in the semiconductor device shown in figure 1 are assigned with the same reference numerals and the description is omitted here.

The hysteresis comparator 6 outputs a high detected signal Y1 when the difference between the reference voltage and the power supply voltage which are two input terminals (input terminal N3 and N4) is larger than the hysteresis width (largeness of the voltage variation).

A description is given of an operation of the semiconductor device constructed as described above. Figure 4 is a timing chart for exemplifying the operation of the semiconductor device shown in figure 3.

In figure 4, first of all, a power supply voltage VDD is applied to the power supply terminal 4, and a reference voltage VREF is applied to the reference voltage input terminal 5. Then, the voltages which are inputted to the input terminal N3 and the N4, respectively are made equal to each other by the resister element 2.

Next, it is supposed that a positive side voltage variation is generated at the power supply voltage VDD from time

t1 to time t2. Then, the voltage variation amount is capacitance-coupled by the capacitance element 3, and thereby the voltage which is inputted from the input terminal N3 to the hysteresis comparator 6 also varies to become a voltage larger than the reference voltage VREF. However, since the voltage difference is smaller than the hysteresis width which is set at the hysteresis comparator 6, the hysteresis comparator 6 will not amplify the voltage difference, and as a result, the detected signal Y1 remains being at low level.

Next, it is supposed that a positive side voltage variation which is larger than the hysteresis width which is set at the hysteresis comparator 6 is generated at the power supply voltage VDD during a time period from time t3 to time t4. In this case, the voltage variation component is capacitance-coupled by the capacitance element 3, and thereby the voltage at the input terminal N3 of the hysteresis comparator 6 varies to become a voltage higher than the reference voltage VREF. Then, the detected signal Y1 of this high level is inputted to the reset part (not shown), and this reset part stops the operation of the whole system including the semiconductor device.

As described above, according to the semiconductor device of the second embodiment, the voltage variation from the state where the reference voltage value and the power supply voltage value are made equal to each other by the resister element 2,

is detected by the hysteresis comparator 6. Thereby, the voltage variation can be detected without depending on the power supply voltage before the voltage variation in the power supply voltage should arise. As a result, with relative to the prior art semiconductor device, parameters which should be taken into considerations on designing are reduced, thereby the circuit design is eased. Further, even if a voltage variation which is smaller than the hysteresis width established in the hysteresis comparator 6 is generated, the detected signal Y1 would not become high level. Thereby, it may not arise that the variation in the power supply voltage which does not affect on the operation of the semiconductor device should erroneously be detected as abnormal voltage variation.

While in the above-described second embodiment, an operation of detecting the positive side voltage variation is described, by making the polarity of the input terminal N3 and the input terminal N4 of the hysteresis comparator 6 reverse to each other, i.e., by making the input terminal N3 - terminal and the input terminal N4 + terminal, the voltage variation at negative side can be detected.

(Embodiment 3)

A third embodiment of the present invention will be described with reference to figures 5 and 6. Figure 5 is a diagram illustrating a circuit construction of a semiconductor device according to the third embodiment of the present

invention. The components similar to those in the semiconductor device shown in figure 3 are assigned with the same reference numerals.

In the semiconductor devices according to the first and the second embodiment, only either of the voltage variations at the positive side and the negative side is detected. Accordingly, the semiconductor device according to the third embodiment provides a construction in which both of the positive side and negative side voltage variations are detected.

The semiconductor device shown in figure 5 includes hysteresis comparators 6 and 7, the resister elements 2 and 8, the capacitance elements 3 and 9, and the logic OR circuit 10. The hysteresis comparator 6 has input terminals (input terminal N3 and N4) and receives the reference voltage and the power supply voltage as at its inputs to compare those. The hysteresis comparator 7 has input terminals (input terminal N5 and N6) and receives the reference voltage and the power supply voltage as at its inputs to compare those. Here, the polarity of its inputs which receive the power supply voltage and the reference voltage are made reverse to those in the hysteresis comparator 6. The resister element 2 connects the signal line L3 connected to the input line N3 of the hysteresis comparator 6 and the signal line L4 connected to the input terminal N4 of the hysteresis comparator 6. The resister element 8 connects the signal line L5 connected to the input terminal N5 of the

hysteresis comparator 7 and the signsal line L6 connected to the input terminal N6 of the hysteresis comparator 7. The capacitance element 3 has its one side end which is connected to the power supply terminal 4 and its other side end which is connected to one side input terminal (input terminal N3) of the hysteresis comparator 6. The capacitance element 9 has its one side end which is connected to the power supply terminal 4 and its other side end which is connected to one side input terminal (input terminal N6) of the hysteresis comparator 7. A logic OR circuit 10 takes a logic OR operation of detected signals Y1, Y2 which are outputted from the hysteresis comparators 6 and 7, to output a detected signal Y3.

The operation of the semiconductor device constructed as above, will be described with reference to figure 6. Figure 6 is a timing chart exemplifying the operation of the semiconductor device shown in figure 5.

In figure 6, first of all, at time t0, a power supply voltage VDD is applied to the power supply voltage terminal 4, and a reference voltage VREF is applied to the input terminal 5 of the reference voltage.

Next, it is supposed that a positive side voltage variation which is larger than the hysteresis width which is set at the hysteresis comparator 6 is generated at the power supply voltage VDD during from time t1 to time t2. Then, the voltage variation component is capacitance-coupled by the

capacitance element 3, and thereby, the voltage which is inputted to the input terminal N3 of the hysteresis comparator 6 also varies to become a voltage higher than the reference voltage VREF. This voltage difference is amplified by the hysteresis comparator 6 to make the detected signal Y1 transit from low level to high level. Then, the logic OR circuit 10 outputs a high level detected signal Y3. This high level detected signal Y3 is inputted to the reset section (not shown), and this reset section stops the operation of the whole system including the semiconductor device at time t3. Accordingly, the voltage becomes 0 V at time t3.

Next, the power supply voltage is again risen at time t4. At time t4, the power supply voltage VDD is applied to the power supply terminal 4 and the reference voltage VREF 3 is applied to the input terminal for a reference voltage.

Next, when a voltage variation at negative side which is larger than the hysteresis width which is set at the hysteresis comparator 7 is risen at the power supply voltage VDD during a period from time t5 to time t6, the voltage variation is capacitance-coupled by the capacitance element 9, and thereby the voltage at the input terminal N5 of the hysteresis comparator 7 becomes a voltage lower than the reference voltage VREF. This voltage difference is amplified by the hysteresis comparator 7 to make the detected signal Y2 transit from low level to high level. Then, the logic OR circuit 10 outputs a

high level detected signal Y3. This high level detected signal Y3 is inputted to the reset section (not shown) and this reset section stops the operation of the whole system including the semiconductor device.

As described above, according to the semiconductor device of the third embodiment of the present invention, the voltage variations at both of the positive side and the negative side from the state where the reference voltage value and the power supply voltage value are made equal to each other by the resister element 2, 8 are detected by the hysteresis comparator 6, 7, respectively. Thereby, the voltage variations at the positive side and the negative side can be detected without depending on the power supply voltage before the power supply voltage variation. As a result, with relative to the prior art semiconductor device, parameters which should be taken into considerations on designing are reduced, thereby the circuit design is eased. Further, even if voltage variations at positive side and negative side which are smaller than the hysteresis widths established in the hysteresis comparator 6, 7, respectively, are generated, the detected signal Y3 would not become high level. Thereby, it may not arise that the variations in the power supply voltages which do not affect on the operation of the semiconductor device should erroneously be detected as abnormal voltage variations.

While in the above-described third embodiment, a case

where a hysteresis comparator is provided, a normal comparator shown in figure 1 may be employed, in place of a hysteresis comparator.

(Embodiment 4)

A fourth embodiment of the present invention will be described with reference to figures 7 and 8. Figure 7 is a diagram illustrating a circuit construction of a semiconductor device according to the fourth embodiment of the present invention. The semiconductor device shown in figure 7, comprises the semiconductor device shown in figure 1 being provided with a voltage variation detection circuit which comprises resister elements 12 and 13 and a comparator 11 having two input terminals, and a logic OR circuit 14.

The resister elements 12 and 13 divide the power supply voltage. The comparator 11 receives the divided power supply voltage from the one side input terminal N7 and receives the reference voltage from the other side input terminal N8.

The operation of the semiconductor device constituted as above will be described with reference to figure 8. Figure 8 is a timing chart for exemplifying the operation of the operation of the semiconductor device shown in figure 7.

In figure 8, at time t0, a power supply voltage VDD is applied to the power supply terminal 4, and a reference voltage is applied to an input terminal for reference voltage 5.

Next, when it is supposed that a positive side voltage

variation has occurred at the power supply voltage VDD from t1 to t2, the voltage variation then is capacitance coupled by a capacitance element 3, and thereby, the voltage that is inputted to the input terminal N1 of the comparator 1 varies to become a higher voltage than the reference voltage VREF. This voltage difference is amplified by the comparator 1 and the detected signal Y1 transits from low level to high level. Thereby, a high level detected signal Y5 is outputted from the logic OR circuit 14. The high level detected signal Y5 is inputted to the reset section (not shown), and the reset section stops the operation of the whole system including the semiconductor device at time t3. That is, the voltage becomes 0 V at time t3. On the other hand, since the voltage which is inputted to the input terminal N7 of the comparator 11 is divided by the resister elements 12 and 13, the steep voltage variation from time t1 to time t2 cannot be detected by the comparator 11.

Next, the power supply voltage is again risen up at time t4. Then, the power supply voltage VDD is applied to the power supply voltage terminal 4, and a reference voltage VREF is applied to the input terminal for reference voltage 5.

Next, when it is supposed that the voltage VDD gradually rises up from time t4 to time t5, the power supply voltage which is divided by the resister elements 12 and 13 also rises up, to become a voltage higher than the reference voltage VFF. This voltage difference is amplified by the comparator 11 and the

detected signal Y4 transits from low level to high level. Thereby, a high level detected signal Y5 is outputted from the logic OR circuit 14, to be inputted to the reset section. Besides, the power supply voltage and the reference voltage which are inputted to the comparator 1 are made the same voltages by the resister element 2, and therefore, the comparator 1 cannot detect the smooth voltage change which arises from time t4 to time t5.

As described above, the semiconductor device according to the fourth embodiment of the present invention, the voltage variation from the state where the reference voltage value and the power supply voltage value are made the same values by the resister element 2 is detected, and therefore, it is possible to detect a steep voltage variation can be detected without dependent on the power supply voltage value before the voltage variation arises. Consequently, with relative to the prior art semiconductor device, parameters which should be taken into considerations on designing are reduced, and the circuit design is eased. Further, since the resister elements 12 and 13, and the comparator 11 which compares the divided voltage and the reference voltage are provided, a smooth voltage variation can also be detected.

While in the above-described fourth embodiment a case where the voltage variation detecting circuit comprising the comparator 11 and the resister elements 12 and 13 are added to

the semiconductor device of the first embodiment, the present invention is not limited thereto, and the voltage variation detecting circuit may be provided in the semiconductor device of the second embodiment and the third embodiment.

Further, when the voltage variation at the negative side is to be detected, the polarities of the input terminals N1, N2, and N7, N8 of the comparator 1 and 11 may be reversed respectively.

(Embodiment 5)

A fifth embodiment of the present invention will be described with reference to figures 9 and 10. Figure 7 is a diagram illustrating a circuit construction of a semiconductor device according to the fifth embodiment of the present invention. The semiconductor device shown in figure 9, comprises the semiconductor device shown in figure 1 being provided with a switching section 15 and a control section 19.

The switching section 15 includes an inverter 16, a p channel transistor 17, and an n channel transistor 18. The output of the inverter 16 is connected to the gate of the p channel transistor 17. The sources of the p channel transistor 17 and the n channel transistor 18 are connected to the input IN1 and the drains thereof are connected to the input terminal N1 of the comparator 1. The switching section 15 constituted as above switches the power supply voltage value which is inputted to the input terminal N1 of the comparator 1 to an

arbitrary value, that is, an arbitrary power supply voltage value which is inputted to the input terminal IN1.

The control section 19 makes the switching section 15 operate by making a test (TEST) signal high, and receives the detected signal Y1 of the comparator 1 to detect as to whether that signal is activated or not.

For example, the control section 19 makes the TEST signal high each time when the power supply voltage of the semiconductor device is turned on, and then the switching section 15 makes the voltage value which is inputted to the input terminal N1 higher than the reference voltage value. Then, whether the comparator 1 has detected that voltage difference and outputted a high level detected signal Y1 or not, is detected by the control section 19.

By constituting the semiconductor device as described above, it is possible to confirm whether the comparator 1 is operating normally or not.

The operation of the semiconductor device constituted as described above will be described with reference to figure 10. Figure 10 shows a timing chart for explaining the operation of the semiconductor device.

First of all, at time t0, a power supply voltage VDD is applied to the power supply terminal 4, and a reference voltage is applied to an input terminal for reference voltage 5. Then, the voltage which is inputted to the input terminals N1 and N2

of the comparator 1 are made equal to each other by the resister element 2.

Next, when the control section 19 makes the test signal which is inputted to the switching section 15 from a low level to a high level at time t1, the p channel transistor 17 and the n channel transistor 18 are turned on, and an arbitrary voltage which is inputted to the input terminal IN1 (hereinafter referred to as "an arbitrary voltage IN1"), i.e., a voltage which is higher than the reference voltage VREF is inputted to the input terminal N1 of the comparator 1. Then, if the comparator 1 is operating normally, the voltage difference between the reference voltage VREF and the arbitrary voltage IN1 is amplified by the comparator 1 and the detected signal Y1 transits from low level to high level. Whether the detected signal Y1 has become high level accompanying that the voltage of the input terminal N1 has become a higher voltage than the reference voltage VREF is confirmed by the control section 19 by inputting the detected signal Y1.

As described above, the semiconductor device of the fifth embodiment of the present invention is provided with a switching section 15 which makes an arbitrary voltage inputted to a terminal for receiving the power supply voltage VDD in the comparator, and thereby it can detect whether the comparator is normally operating or not.

While in this fifth embodiment a case where the voltage

which is inputted to the input terminal N1 by the switching section 15 is switched to a voltage higher than the reference voltage, the present invention is not limited thereto. For example, it may be possible to make the input terminal N1 - terminal, and the input terminal N2 + terminal, and switch the voltage which is inputted to the input terminal N1 to a voltage lower than the reference voltage.

While in the fifth embodiment the control section 19 in the semiconductor device makes the TEST signal high thereby to operate the switching section 15, and receive the detected signal Y1 of the comparator 1 as its input to detect where that signal is activated or not, the present invention is not limited thereto. For example, an external apparatus may control the switching section 15 to make the detected signal Y1 of the comparator 1 inputted to the control section to detect whether the signal is activated or not.

While in the fifth embodiment the semiconductor device of the first embodiment is provided the switching section 15 and the control section 19, the present invention is not limited thereto. For example, the semiconductor device shown in the second to fourth embodiment may be additionally provided with the switching section 15 and the control section 19. Then, the value of the power supply voltage which is inputted to the one-side input terminal of the respective comparators are switched to an arbitrary voltage by the switching section 15.

Further, while in the above-described second to fourth embodiment the resister elements are made those which connect two signal lines which are connected to the two input terminals of the comparator with each other, the two input terminals of the comparator may be connected to each other via only one of the two signal lines, or the two input terminals may be directly connected to each other.

APPLICABILITY IN INDUSTRY

The semiconductor device according to the present invention can detect a steep change of the voltage difference between the power supply voltage and the ground voltage, and therefore, it is suitable in being applied in an LSI which can take a countermeasure against attacks to the semiconductor device such as data falsification or unjustified reading out from the outside.